WHAT IS CLAIMED:

1. An integrated circuit device comprising:

a gate electrode on an active region of an integrated circuit device and on a field isolation layer adjacent to the active region;

a source region and a drain region in the active region on alternate sides of the gate electrode; and

at least one buried insulation layer beneath the drain region or the source region.

2. An integrated circuit device according to Claim 1 further comprising:

a channel silicon layer covering the buried insulation layer in the active region, wherein the source/drain regions are disposed in the channel silicon layer.

3. An integrated circuit device according to Claim 2 wherein the channel silicon layer comprises epitaxially grown single crystalline silicon.

4. An integrated circuit device of Claim 1 wherein the gate electrodes cross top sides of the active region.

5. An integrated circuit device of Claim 4 wherein the top levels of the field isolation layers are lower than top surfaces of the active regions.

6. An integrated circuit device of Claim 4 wherein the gate electrodes fill grooves at boundaries between the active regions and the field isolation layers that expose top sides of the active regions.

7. An integrated circuit device of Claim 6 further comprising:

a recessed liner layer beneath the field isolation layer, wherein inner sides of the grooves include sides of the active regions and the top sides of the field isolation layers adjacent to the top sides of the active regions and the bottom of the grooves defined by the recessed liner layers.

8. An integrated circuit device of Claim 1 wherein the buried insulation

layer comprise a thermal oxide layer.

9. An integrated circuit device of Claim 1 wherein the buried insulation layer and the field isolation layers comprise the same material.

10. An integrated circuit device of Claim 1 wherein the buried insulation layer contacts a bottom surface of the drain region.

11. An integrated circuit device of Claim 1 wherein the buried insulation layer includes at least one vacancy.

12. A method of fabricating an integrated circuit device, comprising:

forming a gate electrode on an active region of an integrated circuit device and on a field isolation layer adjacent to the active region;

forming a source region and a drain region in the active region on alternate sides of the gate electrode; and

forming at least one buried insulation layer beneath the source region or the drain region.

13. A method according to Claim 12 further comprising:

a channel silicon layer between the source/drain regions and above the buried insulation layer.

14. A method of fabricating an integrated circuit device, comprising:

forming at least one passivation layer in a predetermined region of an integrated circuit substrate;

forming a channel silicon layer on the substrate including the passivation layer;

patterning the channel silicon layer and the substrate to expose sides of the passivation layer and to forming a trench defining an active region;

selectively removing the exposed passivation layer to form a vacant space; and

forming a buried insulation layer in the vacant space and forming a field isolation layer in the trench.

15. A method of according to Claim 14 wherein the passivation layer and the channel silicon layer are formed by ultra-high vacuum chemical vapor deposition or low-pressure chemical vapor deposition.

16. A method according to Claim 14 wherein the passivation layer comprises a material having an etch selectivity relative to the substrate and the channel silicon layer.

17. A method according to Claim 14 wherein forming a passivation layer comprises:

forming a mask layer exposing the predetermined region in the substrate;

etching the exposed region through the mask layer to form at least one shallow trench in the substrate;

forming the passivation layer in the shallow trench; and

removing the mask layer, wherein the passivation layer comprises epitaxially grown silicon-germanium.

18. A method according to Claim 17 wherein the channel silicon layer comprise epitaxially grown single crystalline silicon on the passivation layer and the substrate.

19. A method according to Claim 14 wherein forming a buried insulation layer and a field isolation layer comprises:

depositing the field isolation layer to fill the vacant space and the trench; and

planarizing the field isolation layer, wherein a portion of the field isolation layer fills the vacant space to form the buried insulation layer.

20. A method according to Claim 19 further comprising:

forming a thermal oxide layer in the vacant space and the trench prior to depositing the field isolation layer, wherein the thermal oxide layer in the vacant space and the field isolation layer form the buried insulation layer and the thermal oxide layer in the trench forms a sidewall oxide layer.

21. A method according to Claim 14 wherein forming a buried insulation

layer and the field isolation layer comprises:

forming the buried insulation layer to fill the vacant space;

depositing the field isolation layer to fill the trench; and

planarizing the field isolation layer to within the trench, wherein the buried insulation layer comprises a thermal oxide.

22. A method according to Claim 21 wherein forming the buried insulation layer comprises thermally oxidizing the substrate containing the vacant space and the trench to form the buried insulation layer filling the vacant space and a sidewall oxide layer in the trench.

23. A method according to Claim 14 further comprising performing the following steps after forming the buried insulation layer and the field isolation layer:

forming a gate electrode on the active region and the field isolation layer; and

forming impurity diffusion layers in the active regions on both sides of the gate electrode to provide a source and a drain region, wherein at least one of the source and drain regions is on the buried insulation layer.

24. A method according to Claim 23 further comprising performing the following steps before forming the gate electrode:

recessing the field isolation layer to expose top sides of the active region, wherein the gate electrode crosses top and sides of the active region.

25. A method according to Claim 23 further comprising performing the following steps before forming the gate electrode:

forming a groove exposing top sides of the active region at a boundary between the field isolation layer and the active region, wherein the gate electrode fills the groove.

26. A method according to Claim 25 wherein forming s groove comprises:

depositing a liner layer in the trench;

depositing a field isolation layer on the liner layer, filling the trench;

planarizing the field isolation layer the liner layer; and

selectively recessing the liner layer to disclose the top sides of the active

region, wherein the liner layer comprises an insulation material having an etch selectivity relative to the field isolation layer.

27. A method according to Claim 14 wherein the buried insulation layer includes at least one vacancy therein.